REMARKS

In the last Office Action, the Examiner objected to the drawings under 37 C.F.R. §1.83(a) as failing to show the microcomputer recited in claim 2. Claims 1 and 2 were rejected 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,520,336 to Eguchi et al. ("Eguchi"). Claims 3-6 were rejected under 35 U.S.C. §103(a) as being unpatentable over Eguchi in view of U.S. Patent No. 5,017,856 to Johnson Jr. Additional art was cited of interest.

In accordance with the present response, the specification has been suitably revised to correct informalities, provide antecedent basis for the claim language, and to bring it into better conformance with U.S. practice. Original independent claim 1 has been amended to further patentably distinguish from the prior art of record. Original claim 1 has been further amended in formal respects to improve the wording and bring it into better conformance with U.S. practice. Original claims 2-6 have been canceled without prejudice or admission. New claims 7-21 have been added to provide a fuller scope of coverage. A new abstract which more clearly reflects the invention to which the amended and new claims are directed has been substituted for the original abstract.

In view of the cancellation of claim 2, the objection to the drawings under 37 C.F.R. §1.183(a) has been rendered moot.

Applicant requests reconsideration of his application in light of the foregoing amendments and the following discussion.

BRIEF SUMMARY OF INVENTION

The present invention is directed to a battery pack with a remaining battery power calculating function (hereinafter "smart battery pack").

Fig. 5 shows a conventional smart battery pack having a plus side terminal 11, a minus side terminal 12, terminals 13 and 14 for communicating with an electronic device, a secondary battery 10, a protective circuit 1 for protecting the secondary battery 10, a circuit 2 for calculating the remaining capacity of the secondary battery 10, a current detection resistor 3 for current detection, and p-channel MOS transistors 4 and 5.

The protective circuit 1 controls ON/OFF of the P-channel MOS transistors 4 and 5 in accordance with the state of the secondary battery 10. The circuit 2 for calculating the remaining capacity of the secondary battery 10 monitors the voltage of the secondary battery 10 as well as the

electric potential on each end of the current detection resistor 3 to measure a charge current and a discharge current. The measurement results are transmitted to the electronic device through the communication terminals 13 and 14 upon request of the electronic device.

The conventional smart battery pack communicates with the electronic device in accordance with the GND reference, that is, with the electric potential of the minus side terminal 12 as the reference. Applicant has discovered that if an N-channel MOS transistor is used on the Lo side of the conventional smart battery pack, the lower side electric potential of the secondary battery serves as the reference electric potential of the circuit for calculating the remaining capacity of the secondary battery, and thus does not match the GND reference electric potential of the electronic device. Accordingly, the battery pack and the electronic device cannot communicate with each other.

When the conventional smart battery pack communicates with the electronic device using the lower electric potential of the electronic device as the reference, a Hi side transistor of the battery pack has to be a P-channel MOS transistor. This is a problem since P-channel transistors in general have poor mobility and characteristics compared to N-channel MOS transistors.

The present invention overcomes the drawbacks of the conventional art. Figs. 1-4 show a smart battery pack according to the present invention embodied in the claims. The smart battery pack has a secondary battery 10 connected to a plus side terminal 11. A protection circuit 21 protects the secondary battery 10 from overcharge and over-discharge. A calculation circuit 22 operating with a minus side terminal 11 as a reference calculates a remaining capacity of the secondary battery 10. An N-channel MOS transistor 24, 25 is connected between the secondary battery 10 and the minus side terminal 12 for controlling charge and discharge of the secondary battery 10 in accordance with a signal from the protection circuit 22.

A level shifter circuit is connected between the calculation circuit 22 and a communication terminal. In one embodiment shown in Fig. 2, the level shifter circuit shifts and electric potential of the minus side terminal 12 to a minus side electric potential of the secondary battery 10. In another embodiment shown in Fig. 4, the level shifter circuit shifts an electric potential of the minus side of the secondary battery 10 to an electric potential of the minus side terminal 12.

By the foregoing construction of the smart battery pack according to the present invention, by providing an N-channel MOS transistor connected between the secondary battery and a minus side terminal of the smart battery pack, the overall operational characteristic and the efficiency of the smart battery pack is improved over the conventional art. This is due to the fact that N-channel MOS transistors have higher mobility and therefore its ON resistance can be reduced more easily as compared to P-channel MOS transistors used in the conventional smart battery packs. Furthermore, by connecting the level shifter circuit between the calculation circuit and a communication terminal used in conjunction with the smart battery pack, communication between the smart battery pack and an electronic device is made possible and with high efficiency because a reference electric potential of the electronic device and a reference electric potential of the smart battery pack are not made different.

TRAVERSAL OF PRIOR ART REJECTION

Claim 1 was rejected under 35 U.S.C. §103(a) as being unpatentable over Eguchi. Applicant respectfully traverses this rejection and submits that the teachings of Eguchi do not disclose or suggest the subject matter recited in amended independent claim 1.

Amended independent claim 1 is directed to a battery pack with a remaining battery power calculating function and requires a secondary battery connected to a plus side terminal, a protective circuit for protecting the secondary battery from overcharge and over-discharge, a calculation circuit operating with a minus side terminal as a reference for calculating a remaining capacity of the secondary battery, an N-channel MOS transistor connected between the secondary battery and the minus terminal for controlling charge and discharge of the secondary battery upon receiving a signal from the protective circuit in order to protect the secondary battery, and a level shifter circuit connected between the circuit and a communication terminal. No corresponding structural combination is disclosed or suggested by the teachings of Eguchi.

Eguchi is directed to a battery protection circuit having a condition detecting circuit which detects a voltage across a secondary cell and compares the detected voltage with a reference voltage to detect an over-discharge condition or an overcharge condition of the secondary cell (Figs. 1-25). However, Eguchi does not disclose or suggest the structural combination of the battery pack recited in amended independent claim 1, including a secondary battery connected to a plus side terminal, and N-channel MOS transistor connected between

the secondary battery and a minus side terminal, and a level shifter circuit connected between a communication terminal and a calculation circuit for calculating the remaining capacity of the secondary battery and a communication terminal.

For example, in Eguchi the battery protection circuit has a discharging power N-channel MOS (NMOS) transistor QD and a charging power NMOS transistor QC (Fig. 3(B)). The transistor QD has a source terminal connected to a negative terminal of a cell Bbat, a gate terminal connected to a terminal D0, and a drain terminal connected to a drain terminal of the transistor QC. The transistor QC has a source terminal connected to a negative terminal Eb-, a gate terminal connected to a terminal OV, and a drain terminal connected to a drain terminal of the transistor QD. Thus, in Eguchi the N-channel MOS transistor is not connected between a secondary battery and a minus side terminal of the battery pack, as required by amended independent claim 1.

Eguchi further discloses a ground level shifter 27 of a charging logic circuit having an input terminal connected to an output terminal of a NOR gate G8, and an output terminal connected to one of input terminals of a NAND gate G10. Thus, the level shifter 27 in Eguchi is not connected between a calculation circuit for calculating the remaining capacity of

the secondary battery and a communication terminal, as required by the level shifter circuit recited in amended independent claim 1.

The amended independent claim 1 is not rendered obvious by Eguchi because Eguchi does not suggest the modifications that would be needed to replicate the claimed invention. In the context of obviousness rejections based upon the purported obviousness of effecting a required modification, the Federal Circuit has held that "[t]he mere fact that the prior art may be modified in [a given] manner ... does not make the modification obvious unless the prior art suggested the desirability of the modification". In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992). There is nothing in Eguchi that would have suggested modifying the protection circuit therein to achieve the structure of the smart battery pack discussed above and recited by amended independent claim 1.

In view of the foregoing, applicant requests that the rejection of claim 1 under 35 U.S.C. §103(a) as being unpatentable over Eguchi has been overcome and should be withdrawn.

Applicant respectfully submits that newly added claims 7-21 also patentably distinguish from the prior art of record.

Claims 7-11 depend on and contain all of the limitations of amended independent claim 1, and, therefore, distinguish from the prior art of record at least in the same manner as claim 1.

New independent claims 12 and 17 are directed to a battery pack with a remaining battery power calculating function. Each of independent claims 12 and 17 requires a secondary battery connected to a plus side terminal, a calculation circuit that uses a minus side electric potential of the secondary battery as a reference to calculate a remaining capacity of the secondary battery, an N-channel MOS transistor connected between the secondary battery and a minus side terminal of the battery pack for controlling charge and discharge of the secondary battery in accordance with a signal from a protection circuit, and a level shifter circuit connected between the calculation circuit and a communication terminal. No corresponding structural and functional combination is disclosed or suggested by the prior art of record as set forth above for amended independent claim 1.

New claims 13-14 and 18-21 depend on and contain all of the limitations of independent claims 12 and 17, respectively, and, therefore, distinguish from the prior art of record at least in the same manner as claims 12 and 17.

In view of the foregoing amendments and discussion, the application is now believed to be in condition for allowance. Accordingly, favorable reconsideration and allowance of the claims are most respectfully requested.

Respectfully submitted,

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